CLAIMS

1. A decision directed phase locked loop circuit, comprising:

a phase detector which receives a sequence of baseband complex samples and current phase estimates and generates phase differences between said baseband complex samples and current phase estimates;

an inner block decoder which decodes said baseband complex samples to generate partial decoder values and decoded data;

a phase error generation circuit which receives said baseband complex samples and said partial decoder values from said inner block decoder and which generates feedback phase error terms based on said baseband complex samples and said partial decoder values, wherein a group of baseband complex samples consisting of the first baseband complex samples received by said phase detector are run backwards through said inner block decoder;

an outer block decoder which receives the associated codewords generated by said inner block decoder and which utilizes and corrects only codewords associated with baseband complex samples after and including the group of baseband complex samples consisting of the first baseband complex samples received by said phase detector;

a loop filter which filters said phase error terms; and

a phase accumulator that updates the current phase estimate on each iteration of the phase locked loop.

2. A decision directed phase locked loop as claimed in claim 1, wherein the baseband complex samples are demodulated from an input modulated signal corresponding to one of a binary phase shift keying (BPSK) modulated signal and a quaternary phase shift keying (QPSK) modulated signal and encoded by a sequence of codewords.

3. A decision directed phase locked loop as claimed in claim 2, wherein said codewords correspond to biorthogonal binary codes.

4. A decision directed phase locked loop as claimed in claim 3, wherein each of said codewords contains four data symbols, and the decode rate for decoding a set of vector pairs of phase stabilized observables corresponds to one quarter of a symbol rate.

5. A decision directed phase locked loop as claimed in claim 4, wherein said inner block decoder comprises a Reed-Muller block decoder.

6. A decision directed phase locked loop as claimed in claim 5, wherein said phase error generation circuit generates said feedback phase error terms based on the composite decoded codeword phase error relative to reference.

7. A decision directed phase locked loop as claimed in claim 6, wherein said current phase estimate is updated at one quarter the symbol rate.

8. A decision directed phase locked loop as claimed in claim 6, wherein said current phase estimate is updated every codeword of four data symbols.

9 A decision directed phase locked loop as claimed in claim 1, wherein said phase detector includes a subtractor for subtracting the incoming phase of said baseband complex samples from the current phase estimate to generate said phase differences.

10. A demodulator for demodulating a modulated signal waveform in a data communication system, comprising:

a phase tracking loop tracking the phase of said modulated signal waveform and having an inner block decoder configured to decode a set of vector pairs of the modulated signal waveform at a decode rate to generate associated codewords and phase estimates, wherein a group of data symbols consisting of the first data symbols of the modulated signal waveform are run backwards through the phase tracking loop; and

an outer block decoder which receives the associated codewords generated by said inner block decoder and which utilizes and corrects only codewords associated with symbols after the group of data symbols consisting of the first data symbols of modulated signal waveform.

11. A demodulator as claimed in claim 10, wherein said inner block decoder comprises a Reed-Muller block decoder.

12. A demodulator as claimed in claim 11, wherein said Reed-Muller block decoder determines the phase error estimate based on the composite decoded codeword phase error relative to reference.

13. A demodulator as claimed in claim 10, wherein said group of data symbols consisting of the first data symbols of modulated signal waveform are stored in the demodulator.

14. A demodulator as recited in claim 10, wherein said outer block decoder comprises a Reed-Solomon block decoder.

15. A demodulator as claimed in claim 10, wherein the modulated signal waveform is a QPSK modulated waveform and the QPSK ambiguity resolution is determined after the group of data symbols is run backwards through the phase tracking loop.

16. A demodulator as claimed in claim 15, wherein the data is rotated based on the QPSK ambiguity resolution.

17. A demodulator as claimed in claim 16, wherein said preselected codewords comprises the first codewords of the set of associated codewords.

18. A communication receiver using a demodulator demodulating a modulated signal waveform from a transmission channel which is encoded by a sequence of codewords, comprising:

a down converter which generates a succession of baseband signal samples of said input modulated signal including an in-phase component and a quadrature-phase component;

a first converter which converts said succession of baseband signal samples of said input modulated signal from a rectangular form into a pair of polar coordinates having an incoming phase;

a phase tracking loop which estimates the phase of said input modulated signal, said phase locked loop comprising:

a comparator which generates a phase difference of said incoming phase of said input modulated signal and an estimated phase;

a second converter which converts said polar coordinates having said phase difference into a set of vector pairs of phase stabilized observables in said rectangular form;

a first block decoder which decodes said set of vector pairs of phase stabilized observables in said rectangular form at a decode rate to generate associated codewords; and

a loop filter which filters said phase error estimate from said block decoder to yield an update of said estimated phase at each codeword,

wherein a group of data symbols consisting of the first data symbols of the modulated signal waveform are run backwards through the phase tracking loop and

a second block decoder which receives the associated codewords generated by said inner block decoder and which utilizes and corrects only codewords associated with symbols after and including the group of data symbols consisting of the first data symbols of modulated signal waveform.

19. A communication receiver as claimed in claim 18, wherein said input modulated signal comprises a phase shift keying modulated signal.

20. A communication receiver as claimed in claim 18, wherein said first block decoder also generates reliability metric results.

21. A communication receiver as claimed in claim 20, wherein said reliability metric results comprise correlation results taken during decoding by said first block decoder.

22. A communication receiver as claimed in claim 20, wherein said second block decoder dynamically selects codewords from said set of associated codewords.

23. A communication receiver as claimed in claim 18, wherein said block decoder comprises a Reed-Muller block decoder.

24. A communication receiver as claimed in claim 23, wherein said Reed-Muller block decoder determines the phase error estimate based on the composite decoded codeword phase error relative to reference.

25. A communication receiver as claimed in claim 24, wherein said second block decoder preselects the codewords from among said set of associated codewords.

26. A communication receiver as claimed in claim 19, wherein said phase locked loop subtracts the incoming phase of said input modulated signal from the estimated phase to generate the phase difference for tracking the input modulated signal.